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| ART UNIT | PAPER NUMBER |
|---|---|
| 2831 | |

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/694,306 | SUTARDJA, SEHAT | |
| | Examiner | Art Unit | |
| | Eric W Thomas | 2831 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-93* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-93* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 66-92 have been renumbered 67-93.Claims 24, 31, 66 are objected to because of the following informalities:

Claim 24, line 24, insert a comma after "terminals"

Claim 31, line 2, change "material" to –materials–.

Claim 66, line 7 change "a" to –the–.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-8, 10-13, 15-17, 23, 63-67, 69, 78 are rejected under 35 U.S.C. 102(b) as being anticipated by Nagakari et al. (US 6,282,079).

FIG. 19A

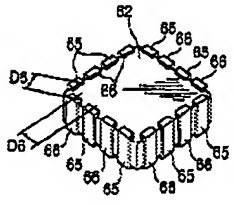


FIG. 19B

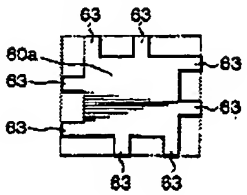
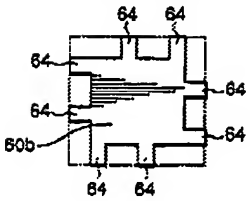


FIG. 19C



Nagakari et al. disclose in fig. 1-5, 19A-19C, a capacitor comprising: m electrode plates; wherein each of said m electrode plates (60a, 60b) are arranged spaced apart in parallel; wherein m is an integer greater than 1; wherein each of said m electrode plates comprises a first extension (63, 64), n first external terminals (65, 66); wherein n is an integer greater than 1; wherein said n first external terminals are arranged on a first common exterior surface of the capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals, wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals, wherein said n first external terminals are arranged at a predefined minimal distance from each other to minimize parasitic inductance (as suggested in col. 14 lines 25-31).

Regarding claim 2, Nagakari et al. disclose that the predefined minimal distance is a minimal distance that prevents crosstalk between the n first external terminals (inherent feature).

Regarding claim 3, Nagakari et al. disclose the n first external terminals are arranged in parallel.

Regarding claim 4, Nagakari et al. disclose n=2 (see fig. 10), and the n first external terminals are arranged in parallel.

Regarding claim 5, Nagakari et al. disclose n=3 (see fig. 17), and the n first external terminals are arranged in parallel and wherein said even one of the n first external terminals is arranged between odd ones of the n first external terminals.

Regarding claim 6, Nagakari et al. disclose a dielectric material is disposed between each of the m electrode plates.

Regarding claim 7, Nagakari et al. disclose the dielectric material is ceramic (col. 7 lines 5-10).

Regarding claim 8, Nagakari et al. disclose exterior ones of the n first external terminals are disposed on the common exterior surface of the capacitor and corresponding side surfaces of the capacitor.

Regarding claim 10, Nagakari et al. (fig. 19A-19C) disclose each of said m electrode plates comprises a second extension, wherein said capacitor comprises s second external terminals, wherein s is an integer greater than 1; wherein said s second external terminals are arranged on a second common exterior surface of the capacitor, wherein said second extensions of said even ones of said m electrode plates are coupled to said even ones of said s second external terminals, wherein said second extensions of said odd ones of said m electrode plates are coupled to odd ones of said s second external terminals.

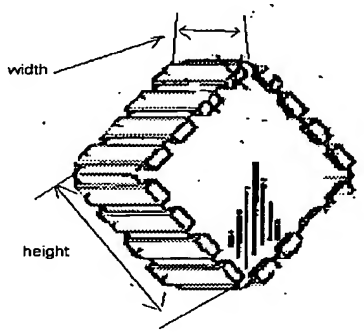
Regarding claim 11, Nagakari et al. disclose the second common exterior surface is arranged opposite to the first common exterior surface.

Regarding claim 12, Nagakari et al. (fig. 19A-19C) disclose wherein each of said m electrodes comprises a second extension, wherein the capacitor comprises s second

external terminals, wherein s is an integer greater than 1; wherein even ones of said s second external terminals are arranged on a third exterior surface of the capacitor, wherein odd ones of said s second external terminals are arranged on a fourth exterior surface of the capacitor, wherein said second extensions of even ones of said m electrode plates are coupled to even ones of said s second external terminals; and wherein said second extensions of odd ones of said m electrode plates are coupled to odd ones of said s second external terminals.

Regarding claim 13, Nagakari et al. disclose the third exterior surface is arranged opposite to the fourth exterior surface.

Regarding claim 15, Nagakari et al. disclose the height of the capacitor is greater than the width.




Regarding claim 16, Nagakari et al. disclose (see fig. 11), a portion of at least one of the n first external terminals wraps around the corner of the capacitor.

Regarding claim 17, Nagakari et al. disclose (as seen in fig. 19 A) the n first external terminals have a bar structure.

Regarding claim 23, Nagakari et al. disclose (see fig. 21 & claim 12), a printed circuit board comprising a plurality of PCB contacts (33), a plurality of capacitor of claim

1 (stacked unit capacitors which are connected in parallel) coupled to the plurality of PCB contacts to facilitate parallel connections of two capacitors.

Regarding claim 63, Nagakari et al. disclose a printed circuit board (see fig. 21 & claim 12), including a plurality of PCB contacts longitudinally arranged in parallel; and a plurality of capacitors (stacked unit capacitors which abuts each other), each of the capacitors are mounted on the PCB, wherein each of the plurality of capacitors comprise the capacitor of claim 1.

Regarding claim 64, Nagakari et al. disclose the second common exterior surface is arranged substantially orthogonal to the first common exterior surface.

Regarding claim 65, Nagakari et al. disclose the third and fourth exterior surfaces are arranged substantially orthogonal to the first common exterior surface.

Regarding claim 66, Nagakari et al. disclose (as seen in fig. 19 A) each of said m electrodes comprises a second extension, wherein the capacitor comprises s second external terminals; wherein s is an integer greater than 1, wherein even ones of said s second external terminals are arranged on a third exterior surface of the capacitor, wherein odd ones of said s second external terminals are arranged on the third exterior surface of the capacitor, wherein said second extensions of even ones of said m electrode plates are coupled to even ones of said s second external terminals, and wherein said second extensions of odd ones of said m electrode plates are coupled to odd ones of said s second external terminals.

Regarding claim 67, Nagakari et al. disclose (as seen in fig. 19A) the odd ones of the s second external terminals are arranged space apart and parallel to the even ones of the s second external terminals.

Regarding claim 69, Nagakari et al. disclose (as seen in fig. 22) an encapsulation (31) encloses a part of the capacitor.

Regarding claim 78, Nagakari et al. disclose the minimal distance is less than 12 mils (as suggested by the table).

5. Claims 24, 41,60, 85, 88, 91 are rejected under 35 U.S.C. 102(b) as being anticipated by Ahiko et al. (US 6,292,351).

Ahiko et al. disclose in fig. 3, 4, a capacitor structure comprising a first capacitor comprising, m electrode plates (1); wherein each of said m electrode plates are arranged spaced apart in parallel, wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension, wherein each of said m electrodes comprises a second extension, n first external terminals, wherein n is an integer greater than 1, wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals, wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals, s second external terminals, wherein s is an integer greater than 1; wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor; wherein said second extension of even ones of said m electrode plates are coupled to even ones of said s second external terminals; wherein

said second extension of odd ones of said m electrode plates are coupled to odd ones of said s second external terminals;

a second capacitor comprising x electrode plates (1), wherein each of said x electrode plates are arranged in parallel, wherein x is an integer greater than 1, wherein each of said x electrodes comprises a third extension, s third external terminals, wherein said s third external terminals are arranged on a third common exterior surface of said second capacitor, wherein said third extension of even ones of said x electrode plates are coupled to even ones of said s third external terminals; wherein said third extension of odd ones of said x electrode plates are coupled to odd ones of said s third external terminals, wherein said second capacitor is mounted on said first capacitor, and wherein said s third external terminals are coupled to corresponding ones of said s second external terminals.

Regarding claim 41, Ahiko et al. dislcose in fig 3,4, a capacitor structure comprising: a first capacitor comprising: m electrode plates, wherein each of said m electrode plates are arranged spaced apart in parallel, wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension and a second extension, n first external terminals; wherein n is an integer greater than 1, wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals; wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals; s second external terminals, wherein s is an integer greater than 0, wherein

said s second external terminals are arranged on a second common exterior surface of the first capacitor, wherein said second extension of even ones of said m electrode plates are coupled to said s second external terminals, a second capacitor (second unit capacitor) comprising: x electrode plates (1); wherein each of said x electrode plates are arranged spaced apart in parallel, wherein x is an integer greater than 1; wherein each of said x electrodes comprises a third extension, s third external terminals, wherein said s third external terminals are arranged on a third common exterior surface of said second capacitor, wherein said third extension of even ones of said x electrode plates are coupled to said s third external terminals, wherein said second capacitor is disposed adjacent to said first capacitor, wherein said s third external terminals are coupled to corresponding ones of said s second terminals.

Regarding claim 60, Ahiko et al. disclose a printed circuit board (see fig. 11) comprising printed circuit board contacts (209a, 209b); and a plurality of capacitors of claim 41 (more than one unit capacitor) coupled to the plurality of PCB contacts to facilitate parallel connections (the unit capacitor stack forms a parallel connection) of at least two capacitors.

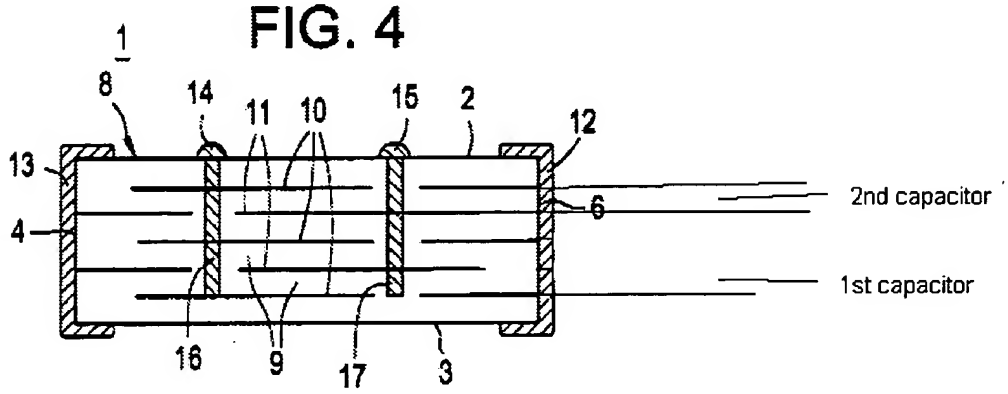
Regarding claim 85, Ahiko et al. disclose a printed circuit board comprising the capacitors of claim 24, wherein the m electrode plates are oriented perpendicular to the printed circuit board.

Regarding claim 88, Ahiko et al. disclose the m electrode plates of the capacitors are oriented perpendicular to the printed circuit board.

Regarding claim 91, Ahiko et al. disclose the m electrode plates of the capacitors are oriented perpendicular to the printed circuit board.

6. Claims 24, 26-29, 31-32, 34-37, 41-43, 45, 47-51, 53, 59, 70, 72-74 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuroda et al. (US 6,594,136).

FIG. 4




Regarding claim 24, Kuroda et al. disclose (as seen in fig. 3A, 3B, 4), a capacitor structure comprising a first capacitor comprising, m electrode plates (10, 11); wherein each of said m electrode plates are arranged spaced apart in parallel, wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension, wherein each of said m electrodes comprises a second extension, n first external terminals, wherein n is an integer greater than 1, wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals, wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals, s second external terminals, wherein s is an integer greater than 1; wherein said s second external

terminals are arranged on a second common exterior surface of the first capacitor; wherein said second extension of even ones of said m electrode plates are coupled to even ones of said s second external terminals; wherein said second extension of odd ones of said m electrode plates are coupled to odd ones of said s second external terminals

a second capacitor comprising x electrode plates, wherein each of said x electrode plates are arranged in parallel, wherein x is an integer greater than 1, wherein each of said x electrodes comprises a third extension, s third external terminals, wherein said s third external terminals are arranged on a third common exterior surface of said second capacitor, wherein said third extension of even ones of said x electrode plates are coupled to even ones of said s third external terminals; wherein said third extension of odd ones of said x electrode plates are coupled to odd ones of said s third external terminals, wherein said second capacitor is mounted on said first capacitor, and wherein said s third external terminals are coupled to corresponding ones of said s second external terminals.

Regarding claim 26, Kuroda et al. disclose the n first external terminals are arranged in parallel, said s second external terminals are arranged in parallel, and wherein said s third external terminals are arranged in parallel.

Regarding claim 27, Kuroda et al. dislcose s=2; wherein said s second external terminals are arranged in parallel and wherein said s third external terminals are arranged in parallel.

Regarding claim 28, Kuroda et al. disclose s=3 (fig. 3A, 3B); wherein said s second external terminals are arranged in parallel and wherein said even one of said s second external terminals is arranged between the odd ones of said s second external terminals and wherein said s third external terminals are arranged in parallel and wherein said even one of said s third external terminals is arranged between the odd ones of said s third external terminals.

Regarding claim 29, Kuroda et al. disclose a first dielectric material is disposed between each of said m electrode plates of said first capacitor, and wherein a second dielectric material is disposed between each of said x electrode plates of said second capacitor.

Regarding claim 31, Kuroda et al. disclose the first and second dielectric materials are the same.

Regarding claim 32, Kuroda et al. disclose the first and second dielectric materials are formed from a ceramic.

Regarding claim 34, Kuroda et al. disclose 34, each of said x electrodes plates comprises a fourth extension, wherein said capacitor comprises u fourth external terminals, wherein u is an integer greater than 1, wherein said u fourth external terminals are arranged on a fourth common exterior surface of said second capacitor; wherein said fourth extensions of said even ones of said x electrode plates are coupled to said even ones of said u fourth external terminals; wherein said fourth extensions of said odd ones of said x electrode plates are coupled to odd ones of said u fourth external terminals.

Regarding claim 35, Kuroda et al. disclose said third common exterior surface is arranged opposite to said fourth common exterior surface.

Regarding claim 36, Kuroda et al. disclose said s second and s third external terminals have a bar structure.

Regarding claim 37, Kuroda et al. disclose said second common exterior surface is arranged substantially orthogonal to the first common exterior surface..

FIG. 3A

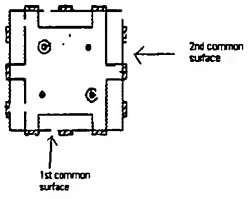
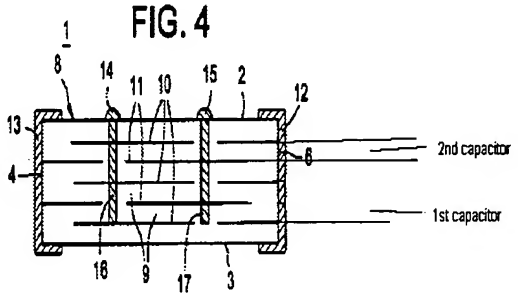



FIG. 4




Regarding claim 41, Kuroda et al. dislcose in fig 3A, 3B, 4, a capacitor structure comprising: a first capacitor comprising: m electrode plates (10, 11), wherein each of said m electrode plates are arranged spaced apart in parallel, wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension and a second extension, n first external terminals (12, 13); wherein n is an integer greater than 1, wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals; wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals; s second external terminals, wherein s is an integer greater than 0, wherein said s second external terminals are arranged on a second common exterior

surface of the first capacitor, wherein said second extension of even ones of said m electrode plates are coupled to said s second external terminals, a second capacitor (second unit capacitor see fig above) comprising: x electrode plates (10,11); wherein each of said x electrode plates are arranged spaced apart in parallel, wherein x is an integer greater than 1; wherein each of said x electrodes comprises a third extension, s third external terminals (12, 13), wherein said s third external terminals are arranged on a third common exterior surface of said second capacitor, wherein said third extension of even ones of said x electrode plates are coupled to said s third external terminals, wherein said second capacitor is disposed adjacent to said first capacitor, wherein said s third external terminals are coupled to corresponding ones of said s second terminals.

Regarding claim 42, Kuroda et al. disclose said n first external terminals are arranged in parallel, wherein said s second external terminals are arranged in parallel; and wherein said s third external terminals are arranged in parallel.

Regarding claim 43, Kuroda et al. disclose s=3; wherein said s second external terminals are arranged in parallel and wherein said even one of said s second external terminals is arranged between the odd ones of said n second external terminals and wherein said s third external terminals are arranged in parallel and wherein said even one of said s third external terminals is arranged between the odd ones of said s third external terminals.

Regarding claim 45, Kuroda et al. disclose a first dielectric material is disposed between each of said m electrode plates of said first capacitor, and wherein a second

dielectric material is disposed between each of said x electrode plates of said second capacitor.

Regarding claim 47, Kuroda et al. disclose said first and second dielectric material are the same.

Regarding claim 48, Kuroda et al. disclose the n first external terminals are arranged in parallel.

Regarding claim 49, Kuroda et al. disclose n=2, wherein said n first external terminals are arranged in parallel.

Regarding claim 50, Kuroda et al. disclose n=3; wherein said n first external terminals are arranged in parallel and wherein said even one of said n first external terminals is arranged between the odd ones of said n first external terminals.

Regarding claim 51, Kuroda et al. disclose the first and second dielectric material comprises ceramic.

Regarding claim 53, Kuroda et al. disclose the n first external terminals have a bar structure.

Regarding claim 59, Kuroda et al. disclose one of the s second external terminals extend from the second common exterior surface to the first common exterior surface of the first capacitor by wrapping around a corner of the first capacitor (fig. 9).

Regarding claim 70, Kuroda et al. disclose the second common exterior surface is arranged substantially orthogonal to the first common exterior surface.

Regarding claim 72, Kuroda et al. disclose an encapsulation (upper ceramic layer) that encloses part of the first and second capacitors.

Regarding claim 73, Kuroda et al. dislcose wherein each of said x electrodes plates comprises a fourth extension, wherein said capacitor comprises u fourth external terminals, wherein u is an integer greater than 1; wherein said u fourth external terminals are arranged on said third common exterior surface of said second capacitor; wherein said fourth extensions of said even ones of said x electrode plates are coupled to said even ones of said u fourth external terminals, wherein said fourth extensions of said odd ones of said x electrode plates are coupled to odd ones of said u fourth external terminals.

Regarding claim 74, Kuroda et al. disclose wherein said second common exterior surface is arranged substantially orthogonal to said first common exterior surface, wherein said third common exterior surface is arranged substantially orthogonal to said fourth common exterior surface.

***Claim Rejections - 35 USC § 103***

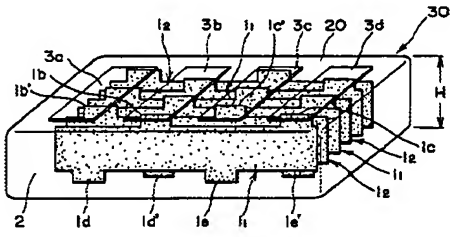
7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1, 23, 63, 81, 84, & 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahiko et al. (US 6,292,351) in view of Nagakari et al. (US 6,282,079).




Ahiko et al. disclose in fig. 1, a capacitor comprising: m electrode plates (1), wherein each of said m electrode plates are arranged spaced apart in parallel; wherein m is an integer greater than 1; wherein each of said m electrode plates comprises a first extension, n first external terminals (3a, 3b), wherein n is an integer greater than 1; wherein said n first external terminals are arranged on a first common exterior surface of the capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals; wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals.

Ahiko et al. disclose the invention except for the n first external terminals are arranged at a predefined minimal distance from each other to minimize parasitic inductance.

Nagakari et al. teach that it is known in the art to minimize parasitic inductance by minimizing the distance between external terminals (as suggested in col. 14 lines 25-31). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the capacitor of Ahiko et al. by minimizing the distances between the external terminals, since such a modification would reduce the parasitic inductance.

Regarding claim 23, Ahiko et al. disclose a printed circuit board (see fig. 11) comprising printed circuit board contacts (209a, 209b); and a plurality of capacitors of claim 1 (more than one unit capacitor) coupled to the plurality of PCB contacts to facilitate parallel connections (the unit capacitor stack forms a parallel connection) of at least two capacitors.

Regarding claim 63, Ahiko et al. disclose a circuit comprising: a printed circuit board including a plurality of PCB contacts longitudinally arranged in parallel (as seen in fig. 11, and 12), and a plurality of capacitors wherein each of said capacitors is arranged abutting with each other and mounted on said PCB (unit capacitors); wherein each of said plurality of capacitors comprises said capacitor of claim 1.

Regarding claim 81, Ahiko et al. disclose a system including a printed circuit board (fig. 16), wherein the m electrode plates of the capacitor are orientated perpendicular to the printed circuit board.

Regarding claim 84, Ahiko et al. disclose the m electrode plates of the capacitors are orientated perpendicular to the printed circuit board.

Regarding claim 93, Ahiko et al. disclose the m electrode plates of the capacitors are orientated perpendicular to the printed circuit board.

10. Claims 1, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Galvagni et al. (US 5,799,379) in view of DuPre et al (US 6,243,253) and Nagakari et al. (US 6,282,079).

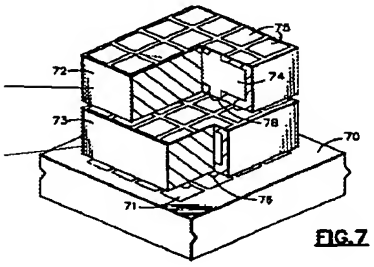


FIG.7

Galvagni et al. disclose (fig. 7) a capacitor comprising electrode plates, each electrode plate has extensions; n first external terminals (75), wherein n is an integer greater than 1; and the n first external terminals are arranged on a first common exterior surface of the capacitor.

Galvagni et al. disclose the claimed invention except for the capacitor comprising: m electrode plates, wherein each of said m electrode plates are arranged spaced apart in parallel; wherein m is an integer greater than 1; wherein each of said m electrode plates comprises a first extension, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals; wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals, wherein the n first external terminals are arranged at a predefined minimal distance from each other to minimize parasitic inductance.

Nagakari et al. teach that it is known in the art to minimize parasitic inductance by minimizing the distance between external terminals (as suggested in col. 14 lines 25-31). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the capacitor of Galvagni et al by minimizing the distances between the external terminals, since such a modification would reduce the parasitic inductance.

DuPre et al. teach (fig. 6) the use of capacitor electrodes having tab portions matching the external terminals of the capacitors of Galvagni et al., it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the capacitors of Galvagni et al, using the electrodes of DuPre, since such a modification would produce a capacitor having electrodes that would connect to the corresponding external electrodes; and would provide electrodes that would cancel inductance.

It should be noted Galvagni et al. as modified by Nagakari et al. and DuPre et al., would form a capacitor structure comprising m electrode plates, wherein each of said m electrode plates are arranged spaced apart in parallel, wherein m is an integer greater than 1; wherein each of said m electrode plates comprises a first extension, n first external terminals, wherein n is an integer greater than 1, wherein said n first external terminals are arranged on a first common exterior surface of the capacitor, wherein said first extension of even ones of said m electrode plates are coupled lo even ones of said n first external terminals, wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals; wherein said n first

external terminals are arranged at a predefined minimal distance from each other to minimize parasitic inductance.

Regarding claim 9, Galvagni et al. as modified by Nagakari et al. and DuPre et al., wherein a first one and a second one of said n first external terminals are arranged in a first row; wherein a third one and a fourth one of said n first external terminals are arranged in a second row; wherein said first one of said n first external terminals is arranged adjacent said second and fourth ones of said n first external terminals and diagonal to said third one of said n first external terminals, wherein said second one of said n first external terminals is arranged diagonal to said fourth one of said n first external terminals.

11. Claims 14, and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagakari et al. (US 6,282,079) in view of DiFonzo et al. (US 6,262,886).

Regarding claim 14, Nagakari et al. disclose the claimed invention except for the capacitor is formed in a housing that encloses at least a part of the capacitor. The capacitor of Nagakari et al. is used in a computer environment.

DiFonzo et al. teach that it is known to use a housing for a computer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the capacitor (computer) of Nagakari et al. in a housing as taught by DiFonzo et al., since such a modification would provide protection for the system of Nagakari et al. (the capacitor Nagakari et al. (as modified by DiFonzo) is enclosed by a housing).

Regarding claim 68, DiFonzo et al. teach the claimed housing. Regarding the limitation, "the housing is formed from an ejection molding process" is a method of forming the device. The method of forming the device is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight.

12. Claim 79 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagakari et al. (US 6,282,079).

Nagakari et al. disclose the claimed invention except for the predefined minimal distance is less than 8 mils.

It would have been an obvious matter of design choice to form the capacitor having a minimal distance of 7.5 mils, since such a modification would have involved a mere change in the size of a component, a change in size is generally recognized as being within the level of ordinary skill in the art. *In re. Rose, 105 USPQ 237 (CCPA 1955).*

13. Claims 25, 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda et al. ~~(US 6,327,134)~~ (US 6,594,136) in view of DiFonzo et al. (US 6,262,886). -ET 9/17/04

Kuroda et al. disclose the claimed invention except for a housing that encloses at least part of the first and second capacitors. Kuroda et al. disclose the capacitors are used in a person computer.

DiFonzo et al. teach that it is known to use a housing for a computer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the capacitors (computer) of Kuroda et al. in a housing as taught by

DiFonzo et al., since such a modification would provide protection for the system of Nagakari et al. (the capacitors Kuroda et al. (as modified by DiFonzo) are enclosed by a housing).

Regarding claim 71, DiFonzo et al. teach the claimed housing. Regarding the limitation, "the housing is formed from an ejection molding process" is a method of forming the device. The method of forming the device is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight.

14. Claims 24, 26-35, and 41-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Galvagni et al. (US 5,799,379) in view of DuPre et al. (US 6,243,253).

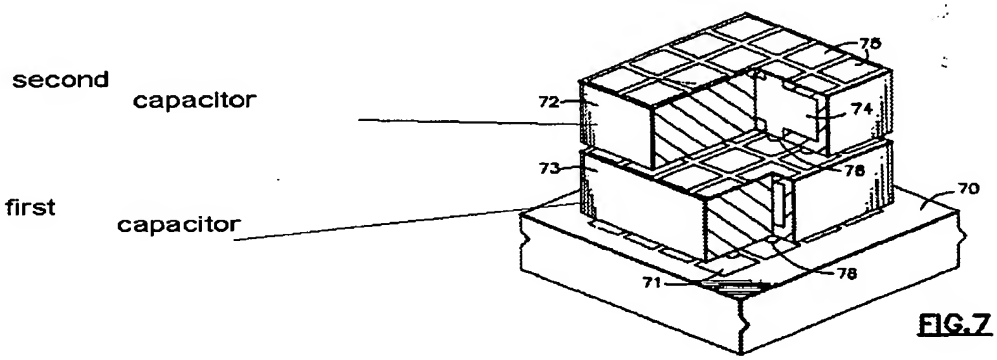



FIG.7

Galvagni et al. disclose a first capacitor and a second capacitor, wherein the first capacitor and second capacitor comprise multiple terminals (75) on first (n first external terminals, wherein n is greater than 1), second (s second external terminals, wherein s is an integer greater than 1), third (s third external terminal) and fourth common side surfaces, the second capacitor is mounted on the first capacitor; and wherein said s

third external terminals are coupled to corresponding ones of said s second external terminals.

Galvagni et al. disclose the claimed invention except for the first capacitor comprising, m electrode plates; wherein each of said m electrode plates are arranged spaced apart in parallel, wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension, wherein each of said m electrodes comprises a second extension, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals, wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals; wherein said second extension of even ones of said m electrode plates are coupled to even ones of said s second external terminals; wherein said second extension of odd ones of said m electrode plates are coupled to odd ones of said s second external terminals; the second capacitor comprising x electrode plates, wherein each of said x electrode plates are arranged in parallel, wherein x is an integer greater than 1, wherein each of said x electrodes comprises a third extension, wherein said third extension of even ones of said x electrode plates are coupled to even ones of said s third external terminals; wherein said third extension of odd ones of said x electrode plates are coupled to odd ones of said s third external terminals.

DuPre et al. (fig. 6) teach the use of capacitor electrodes having tab portions matching the external terminals of the capacitors of Galvagni et al., it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the capacitors of Galvagni et al, using the electrodes of DuPre, since such a

modification would produce a capacitor having electrodes that would connect to the corresponding external electrodes; and would provide electrodes that would cancel inductance.

It should be noted Galvagni et al. as modified by DuPre et al., would form a capacitor structure comprising a first capacitor comprising, m electrode plates; wherein each of said m electrode plates are arranged spaced apart in parallel, wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension, wherein each of said m electrodes comprises a second extension, n first external terminals, wherein n is an integer greater than 1, wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals, wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals, s second external terminals, wherein s is an integer greater than 1; wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor; wherein said second extension of even ones of said m electrode plates are coupled to even ones of said s second external terminals; wherein said second extension of odd ones of said m electrode plates are coupled to odd ones of said s second external terminals

a second capacitor comprising x electrode plates, wherein each of said x electrode plates are arranged in parallel, wherein x is an integer greater than 1, wherein each of said x electrodes comprises a third extension, s third external terminals,

wherein said s third external terminals are arranged on a third common exterior surface of said second capacitor, wherein said third extension of even ones of said x electrode plates are coupled to even ones of said s third external terminals; wherein said third extension of odd ones of said x electrode plates are coupled to odd ones of said s third external terminals, wherein said second capacitor is mounted on said first capacitor, and wherein said s third external terminals are coupled to corresponding ones of said s second external terminals.

Regarding claim 26, Galvagni et al. as modified by DuPre et al., disclose the n first external terminals are arranged in parallel, said s second external terminals are arranged in parallel, and wherein said s third external terminals are arranged in parallel.

Regarding claim 27 Galvagni et al. as modified by DuPre et al., disclose s=2; wherein said s second external terminals are arranged in parallel and wherein said s third external terminals are arranged in parallel.

Regarding claim 28, Galvagni et al. as modified by DuPre et al., disclose s=3; wherein said s second external terminals are arranged in parallel and wherein said even one of said s second external terminals is arranged between the odd ones of said s second external terminals and wherein said s third external terminals are arranged in parallel and wherein said even one of said s third external terminals is arranged between the odd ones of said s third external terminals.

Regarding claim 29, Galvagni et al. as modified by DuPre et al., disclose a first dielectric material is disposed between each of said m electrode plates of said first

capacitor, and wherein a second dielectric material is disposed between each of said x electrode plates of said second capacitor.

Regarding claim 30, Galvagni et al. as modified by DuPre et al., disclose the claimed invention except for the ceramic of the first and second capacitors are different. It is well known (using multiple capacitors in the electronic industry) to use capacitors having different ceramic materials (dielectric) wherein the capacitors are connected together. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the system of Li et al., using two capacitors having the same structure but different in dielectric composition, since such a modification would provide a capacitor structure having a total capacitance that would be different than the total capacitance of a system having multiple like capacitors.

Regarding claim 31, Galvagni et al. as modified by DuPre et al., disclose the first and second dielectric materials are the same.

Regarding claim 32, Galvagni et al. as modified by DuPre et al., disclose the first and second dielectric materials are formed from a ceramic.

Regarding claim 33, Galvagni et al. as modified by DuPre et al. (see fig. 7), disclose a first one and a second one of said s second external terminals are arranged in a first row; wherein a third one and a fourth one of said s second external terminals are arranged in a second row, wherein said first one of said s second external terminals is arranged adjacent to said second and fourth ones of said s second external terminals and diagonal to said third one of said s second external terminals, wherein said second one of said s second external terminals is arranged diagonal to said fourth one of said s

second external terminals; wherein a first one and a second one of said s third external terminals are arranged in a first row; wherein a third one and a fourth one of said s third external terminals are arranged in a second row; wherein said first one of said s third external terminals is arranged adjacent to said second and fourth ones of said s third external terminals and diagonal to said third one of said s third external terminals, and wherein said second one of said s third external terminals is arranged diagonal to said fourth one of said s third external terminals.

Regarding claim 34, Galvagni et al. as modified by DuPre et al., disclose each of said x electrodes plates comprises a fourth extension, wherein said capacitor comprises u fourth external terminals, wherein u is an integer greater than 1, wherein said u fourth external terminals are arranged on a fourth common exterior surface of said second capacitor; wherein said fourth extensions of said even ones of said x electrode plates are coupled to said even ones of said u fourth external terminals; wherein said fourth extensions of said odd ones of said x electrode plates are coupled to odd ones of said u fourth external terminals.

Regarding claim 35, Galvagni et al. as modified by DuPre et al., disclose said third common exterior surface is arranged opposite to said fourth common exterior surface.

Regarding claim 41, Galvagni et al. disclose a first capacitor and a second capacitor, wherein the first capacitor and second capacitor comprise multiple terminals (75) on first (n first external terminals, wherein n is greater than 1), second (s second external terminals, wherein s is an integer greater than 1), third (s third external

terminal) and fourth common side surfaces, the second capacitor is mounted on the first capacitor; and wherein said s third external terminals are coupled to corresponding ones of said s second external terminals.

Galvangni et al. disclose the claimed invention except for except the first capacitor comprising: m electrode plates, wherein each of said m electrode plates are arranged spaced apart in parallel, wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension and a second extension, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals; wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals; wherein said second extension of even ones of said m electrode plates are coupled to said s second external terminals, the second capacitor comprising: x electrode plates; wherein each of said x electrode plates are arranged spaced apart in parallel, wherein x is an integer greater than 1; wherein each of said x electrodes comprises a third extension, wherein said third extension of even ones of said x electrode plates are coupled to said s third external terminals, wherein said second capacitor is disposed adjacent to said first capacitor, wherein said s third external terminals are coupled to corresponding ones of said s second terminals.

DuPre et al. (fig. 6) teach the use of capacitor electrodes having tab portions matching the external terminals of the capacitors of Galvagni et al., it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the capacitors of Galvagni et al, using the electrodes of DuPre, since such a

modification would produce a capacitor having electrodes that would connect to the corresponding external electrodes; and would provide electrodes that would cancel inductance.

It should be noted Galvagni et al. as modified by DuPre et al., would form would form a capacitor structure comprising: a first capacitor comprising: m electrode plates, wherein each of said m electrode plates are arranged spaced apart in parallel, wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension and a second extension, n first external terminals; wherein n is an integer greater than 1, wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals; wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals; s second external terminals, wherein s is an integer greater than 0, wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor, wherein said second extension of even ones of said m electrode plates are coupled to said s second external terminals, a second capacitor comprising: x electrode plates; wherein each of said x electrode plates are arranged spaced apart in parallel, wherein x is an integer greater than 1; wherein each of said x electrodes comprises a third extension, s third external terminals, wherein said s third external terminals are arranged on a third common exterior surface of said second capacitor, wherein said third extension of even ones of said x electrode plates are coupled to said s third external terminals, wherein said second capacitor is

disposed adjacent to said first capacitor, wherein said s third external terminals are coupled to corresponding ones of said s second terminals.

Regarding claim 42, Galvagni et al. as modified by DuPre et al., disclose said n first external terminals are arranged in parallel, wherein said s second external terminals are arranged in parallel; and wherein said s third external terminals are arranged in parallel.

Regarding claim 43, Galvagni et al. as modified by DuPre et al., disclose s=3; wherein said s second external terminals are arranged in parallel and wherein said even one of said s second external terminals is arranged between the odd ones of said n second external terminals and wherein said s third external terminals are arranged in parallel and wherein said even one of said s third external terminals is arranged between the odd ones of said s third external terminals.

Regarding claim 44, Galvagni et al. as modified by DuPre et al., disclose s=3; wherein said s second external terminals are arranged in parallel and wherein said even one of said s second external terminals is arranged between the odd ones of said n second external terminals and wherein said s third external terminals are arranged in parallel and wherein said even one of said s third external terminals is arranged between the odd ones of said s third external terminals.

Regarding claim 45, Galvagni et al. as modified by DuPre et al., disclose a first dielectric material is disposed between each of said m electrode plates of said first capacitor, and wherein a second dielectric material is disposed between each of said x electrode plates of said second capacitor.

Regarding claim 46, Galvagni et al. as modified by DuPre et al., disclose the claimed invention except for the ceramic of the first and second capacitors are different. It is well known (using multiple capacitors in the electronic industry) to use capacitors having different ceramic materials (dielectric) wherein the capacitors are connected together. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the system of Li et al., using two capacitors having the same structure but different in dielectric composition, since such a modification would provide a capacitor structure having a total capacitance that would be different than the total capacitance of a system having multiple like capacitors.

Regarding claim 47, Galvagni et al. as modified by DuPre et al., disclose said first and second dielectric material are the same.

Regarding claim 48, Galvagni et al. as modified by DuPre et al., disclose the n first external terminals are arranged in parallel.

Regarding claim 49, Galvagni et al. as modified by DuPre et al., disclose n=2, wherein said n first external terminals are arranged in parallel.

Regarding claim 50, Galvagni et al. as modified by DuPre et al., disclose n=3; wherein said n first external terminals are arranged in parallel and wherein said even one of said n first external terminals is arranged between the odd ones of said n first external terminals.

Regarding claim 51, Galvagni et al. as modified by DuPre et al., disclose the first and second dielectric material comprises ceramic.

Regarding claim 52, Galvagni et al. as modified by DuPre et al., disclose n is 4, wherein a first one and a second one of said n first external terminals are arranged in a first row; wherein a third one and a fourth one of said n first external terminals are arranged in a second row; wherein said first one of said n first external terminals is arranged adjacent to said second and fourth ones of said n first external terminals and diagonal to said third one of said n first external terminals, and wherein the second one of the n first external terminals is arranged diagonal to the fourth one of the n first external terminals.

Regarding claim 61, Galvagni et al. disclose a device comprising a first capacitor comprising: n first external terminals (75), wherein n is an integer greater than 1; wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor, s second external terminals (75); wherein s is an integer greater than 1; wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor; a second capacitor comprising: q third external terminals, wherein q is an integer greater than 1, wherein said q third external terminals are arranged on a third common exterior surface of said second capacitor; wherein said second capacitor is disposed abutting and adjacent to said first capacitor. Galvagni et al. disclose the claimed invention except for the electrode structure.

DuPre et al. (fig. 6) teach the use of capacitor electrodes having tab portions matching the external terminals of the capacitors of Galvagni et al., it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the capacitors of Galvagni et al, using the electrodes of DuPre, since such a

modification would produce a capacitor having electrodes that would connect to the corresponding external electrodes; and would provide electrodes that would cancel inductance.

It should be noted that Galvagni et al. as modified by DuPre disclose a device comprising: a first capacitor comprising: m electrode plates; wherein each of said m electrode plates are arranged spaced apart in parallel; wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension, wherein w electrode plates of said m electrode plates comprise a second extension, wherein w is an integer less than m; n first external terminals; wherein n is an integer greater than 1; wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals; wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals; s second external terminals; wherein s is an integer greater than 1; wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor; wherein said second extension of even ones of said w electrode plates are coupled to even ones of said s second external terminals; wherein said second extension of odd ones of said w electrode plates are coupled to odd ones of said s second external terminals, a second capacitor comprising: x electrode plates, wherein each of said x electrode plates are arranged spaced apart in parallel; wherein x is an integer greater than 1, wherein y electrode plates of said x electrode plates comprise a third extension, wherein y is an integer less than x; q third external

terminals, wherein q is an integer greater than 1, wherein said q third external terminals are arranged on a third common exterior surface of said second capacitor; wherein said third extension of even ones of said y electrode plates are coupled to even ones of said q third external terminals, wherein said third extension of odd ones of said y electrode plates are coupled to odd ones of said q third external terminals; wherein said second capacitor is disposed abutting and adjacent to said first capacitor, wherein said even ones of said q third external terminals are coupled to said even ones of said s second terminals; and wherein said odd ones of said q third external terminals are coupled to said odd ones of said s second terminals.

15. Claims 24, 26-30, 31-32, 34-36, 41-43, 45-51, 53, 59, 61-62, 70, 72-74, 77, 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (US 6,636,416) in view of Naito et al. (US 6,072,687).

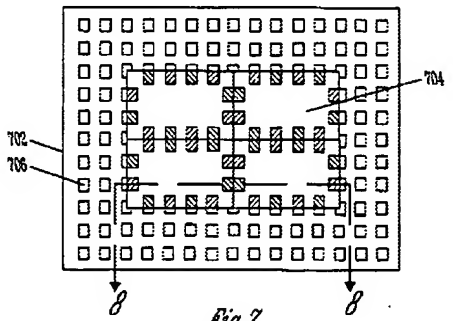


Fig. 7

Li et al. disclose in fig. 7, a capacitor structure comprising: first and second capacitors having 12 terminals.

Li et al. disclose the claimed invention except for the first capacitor comprising, m electrode plates; wherein each of said m electrode plates are arranged spaced apart in parallel, wherein m is an integer greater than 1; wherein each of said m electrodes

comprises a first extension, wherein each of said m electrodes comprises a second extension, n first external terminals, wherein n is an integer greater than 1, wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals, wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals, s second external terminals, wherein s is an integer greater than 1; wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor; wherein said second extension of even ones of said m electrode plates are coupled to even ones of said s second external terminals; wherein said second extension of odd ones of said m electrode plates are coupled to odd ones of said s second external terminals; the second capacitor comprising x electrode plates, wherein each of said x electrode plates are arranged in parallel, wherein x is an integer greater than 1, wherein each of said x electrodes comprises a third extension, s third external terminals, wherein said s third external terminals are arranged on a third common exterior surface of said second capacitor, wherein said third extension of even ones of said x electrode plates are coupled to even ones of said s third external terminals; wherein said third extension of odd ones of said x electrode plates are coupled to odd ones of said s third external terminals, wherein said second capacitor is mounted on said first capacitor, and wherein said s third external terminals are coupled to corresponding ones of said s second external terminals.

Naito et al. teach (fig. 1-3) the use of an improve capacitor having m electrode plates; wherein each of said m electrode plates are arranged spaced apart in parallel, wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension, wherein each of said m electrodes comprises a second extension, n first external terminals, wherein n is an integer greater than 1, wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals, wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals, s second external terminals, wherein s is an integer greater than 1; wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor; wherein said second extension of even ones of said m electrode plates are coupled to even ones of said s second external terminals.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the capacitors of Naito et al. in the system of Li et al., since such a modification would provide a group of capacitors in the system of Li et al.; and would provide a group of capacitors having a reduced series inductance.

*It should be noted Li et al. as combined with Naito et al. would form a capacitor structure comprising a first capacitor comprising, m electrode plates; wherein each of said m electrode plates are arranged spaced apart in parallel, wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension, wherein each of said m electrodes comprises a second extension, n first external terminals,

wherein n is an integer greater than 1, wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals, wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals, s second external terminals, wherein s is an integer greater than 1; wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor; wherein said second extension of even ones of said m electrode plates are coupled to even ones of said s second external terminals; wherein said second extension of odd ones of said m electrode plates are coupled to odd ones of said s second external terminals

a second capacitor comprising x electrode plates, wherein each of said x electrode plates are arranged in parallel, wherein x is an integer greater than 1, wherein each of said x electrodes comprises a third extension, s third external terminals, wherein said s third external terminals are arranged on a third common exterior surface of said second capacitor, wherein said third extension of even ones of said x electrode plates are coupled to even ones of said s third external terminals; wherein said third extension of odd ones of said x electrode plates are coupled to odd ones of said s third external terminals, wherein said second capacitor is mounted on said first capacitor (as illustrated in fig. 7), and wherein said s third external terminals are coupled to corresponding ones of said s second external terminals.

Regarding claim 26, Li et al. as combined with Naito et al. disclose the n first external terminals are arranged in parallel, said s second external terminals are arranged in parallel, and wherein said s third external terminals are arranged in parallel.

Regarding claim 27, Li et al. as combined with Naito et al. disclose s=2; wherein said s second external terminals are arranged in parallel and wherein said s third external terminals are arranged in parallel.

Regarding claim 28, Li et al. as combined with Naito et al. disclose s=3; wherein said s second external terminals are arranged in parallel and wherein said even one of said s second external terminals is arranged between the odd ones of said s second external terminals and wherein said s third external terminals are arranged in parallel and wherein said even one of said s third external terminals is arranged between the odd ones of said s third external terminals.

Regarding claim 29, Li et al. as combined with Naito et al. disclose a first dielectric material is disposed between each of said m electrode plates of said first capacitor, and wherein a second dielectric material is disposed between each of said x electrode plates of said second capacitor.

Regarding claim 30, the modified Li et al. disclose the claimed invention except for the ceramic of the first and second capacitors are different. It is well known (using multiple capacitors in the electronic industry) to use capacitors having different ceramic materials (dielectric) wherein the capacitors are connected together. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the system of Li et al., using two capacitors having the same structure but

different in dielectric composition, since such a modification would provide a capacitor structure having a total capacitance that would be different than the total capacitance of a system having multiple like capacitors.

Regarding claim 31, Li et al. as combined with Naito et al. disclose the first and second dielectric materials are the same.

Regarding claim 32, Li et al. as combined with Naito et al. disclose the first and second dielectric materials are formed from a ceramic.

Regarding claim 34 Li et al. as combined with Naito et al. disclose each of said x electrodes plates comprises a fourth extension, wherein said capacitor comprises u fourth external terminals, wherein u is an integer greater than 1, wherein said u fourth external terminals are arranged on a fourth common exterior surface of said second capacitor; wherein said fourth extensions of said even ones of said x electrode plates are coupled to said even ones of said u fourth external terminals; wherein said fourth extensions of said odd ones of said x electrode plates are coupled to odd ones of said u fourth external terminals.

Regarding claim 35, Li et al. as combined with Naito et al. disclose said third common exterior surface is arranged opposite to said fourth common exterior surface.

Regarding claim 36, Li et al. as combined with Naito et al. disclose said s second and s third external terminals have a bar structure.

Regarding claim 37, Li et al. as combined with Naito et al. disclose said second common exterior surface is arranged substantially orthogonal to the first common exterior surface.

Regarding claim 41, Li et al. disclose a capacitor structure comprising first and second capacitors.

Li et al. disclose the claimed invention except the first capacitor comprising: m electrode plates, wherein each of said m electrode plates are arranged spaced apart in parallel, wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension and a second extension, n first external terminals; wherein n is an integer greater than 1, wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals; wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals; s second external terminals, wherein s is an integer greater than 0, wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor, wherein said second extension of even ones of said m electrode plates are coupled to said s second external terminals, the second capacitor comprising: x electrode plates; wherein each of said x electrode plates are arranged spaced apart in parallel, wherein x is an integer greater than 1; wherein each of said x electrodes comprises a third extension, s third external terminals, wherein said s third external terminals are arranged on a third common exterior surface of said second capacitor, wherein said third extension of even ones of said x electrode plates are coupled to said s third external terminals, wherein said second capacitor is disposed adjacent to said first capacitor, wherein said s third external terminals are coupled to corresponding ones of said s second terminals.

Naito et al. teach the use of a capacitor, wherein the capacitor comprises : m electrode plates, wherein each of said m electrode plates are arranged spaced apart in parallel, wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension and a second extension, n first external terminals; wherein n is an integer greater than 1, wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals; wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals; s second external terminals, wherein s is an integer greater than 0, wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor, wherein said second extension of even ones of said m electrode plates are coupled to said s second external terminals.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the capacitors of Naito et al. in the system of Li et al., since such a modification would provide a group of capacitors in the system of Li et al.; and would provide a group of capacitors having a reduced series inductance.

*It should be noted Li et al. as combined with Naito et al. would form a capacitor structure comprising: a first capacitor comprising: m electrode plates, wherein each of said m electrode plates are arranged spaced apart in parallel, wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension and a second extension, n first external terminals; wherein n is an integer greater than 1,

wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals; wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals; s second external terminals, wherein s is an integer greater than 0, wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor, wherein said second extension of even ones of said m electrode plates are coupled to said s second external terminals, a second capacitor comprising: x electrode plates; wherein each of said x electrode plates are arranged spaced apart in parallel, wherein x is an integer greater than 1; wherein each of said x electrodes comprises a third extension, s third external terminals, wherein said s third external terminals are arranged on a third common exterior surface of said second capacitor, wherein said third extension of even ones of said x electrode plates are coupled to said s third external terminals, wherein said second capacitor is disposed adjacent to said first capacitor, wherein said s third external terminals are coupled to corresponding ones of said s second terminals.

Regarding claim 42, Li et al. as combined with Naito et al. disclose said n first external terminals are arranged in parallel, wherein said s second external terminals are arranged in parallel; and wherein said s third external terminals are arranged in parallel.

Regarding claim 43, Li et al. as combined with Naito et al. disclose s=3; wherein said s second external terminals are arranged in parallel and wherein said even one of said s second external terminals is arranged between the odd ones of said n second

external terminals and wherein said s third external terminals are arranged in parallel and wherein said even one of said s third external terminals is arranged between the odd ones of said s third external terminals.

Regarding claim 45, Li et al. as combined with Naito et al. disclose a first dielectric material is disposed between each of said m electrode plates of said first capacitor, and wherein a second dielectric material is disposed between each of said x electrode plates of said second capacitor.

Regarding claim 46, the modified Li et al. disclose the claimed invention except for the ceramic of the first and second capacitors are different. It is well known (using multiple capacitors in the electronic industry) to use capacitors having different ceramic materials (dielectric) wherein the capacitors are connected together. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the system of Li et al., using two capacitors having the same structure but different in dielectric composition, since such a modification would provide a capacitor structure having a total capacitance that would be different than the total capacitance of a system having multiple like capacitors.

Regarding claim 47, Li et al. as combined with Naito et al. disclose said first and second dielectric material are the same.

Regarding claim 48, Li et al. as combined with Naito et al. disclose the n first external terminals are arranged in parallel.

Regarding claim 49, Li et al. as combined with Naito et al. disclose n=2, wherein said n first external terminals are arranged in parallel.

Regarding claim 50, Li et al. as combined with Naito et al. disclose n=3; wherein said n first external terminals are arranged in parallel and wherein said even one of said n first external terminals is arranged between the odd ones of said n first external terminals.

Regarding claim 51, Li et al. as combined with Naito et al. disclose the first and second dielectric material comprises ceramic.

Regarding claim 53, Li et al. as combined with Naito et al. disclose the n first external terminals have a bar structure.

Regarding claim 59, Li et al. as combined with Naito et al. disclose one of the s second external terminals extend from the second common exterior surface to the first common exterior surface of the first capacitor by wrapping around a corner of the first capacitor.

Regarding claim 70, Li et al. as combined with Naito et al. disclose the second common exterior surface is arranged substantially orthogonal to the first common exterior surface.

Regarding claim 72, Li et al. as combined with Naito et al. disclose an encapsulation (upper ceramic layer) that encloses part of the first and second capacitors.

Regarding claim 73, Li et al. as combined with Naito et al. disclose wherein each of said x electrodes plates comprises a fourth extension, wherein said capacitor comprises u fourth external terminals, wherein u is an integer greater than 1; wherein said u fourth external terminals are arranged on said third common exterior surface of

said second capacitor; wherein said fourth extensions of said even ones of said x electrode plates are coupled to said even ones of said u fourth external terminals, wherein said fourth extensions of said odd ones of said x electrode plates are coupled to odd ones of said u fourth external terminals.

Regarding claim 74, Li et al. as combined with Naito et al. disclose wherein said second common exterior surface is arranged substantially orthogonal to said first common exterior surface, wherein said third common exterior surface is arranged substantially orthogonal to said fourth common exterior surface.

Regarding claim 61, Li et al. disclose a device comprising first and second capacitors.

Li et al. disclose the claimed invention except for the first capacitor comprising, m electrode plates; wherein each of said m electrode plates are arranged spaced apart in parallel; wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension, wherein w electrode plates of said m electrode plates comprise a second extension, wherein w is an integer less than m; n first external terminals; wherein n is an integer greater than 1; wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals; wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals, s second external terminals, wherein s is an integer greater than 1; wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor,

wherein said second extension of even ones of said w electrode plates are coupled to even ones of said s second external terminals, wherein said second extension of odd ones of said w electrode plates are coupled to odd ones of said s second external terminals, the second capacitor comprising: x electrode plates, wherein each of said x electrode plates are arranged spaced apart in parallel; wherein x is an integer greater than 1; wherein y electrode plates of said x electrode plates comprise a third extension, wherein y is an integer less than x; q third external terminals, wherein q is an integer greater than 1, wherein said q third external terminals are arranged on a third common exterior surface of said second capacitor; wherein said third extension of even ones of said y electrode plates are coupled to even ones of said q third external terminals; wherein said third extension of odd ones of said y electrode plates are coupled to odd ones of said q third external terminals; wherein said second capacitor is disposed abutting and adjacent to said first capacitor, wherein said even ones of said q third external terminals are coupled to said even ones of said s second terminals; and wherein said odd ones of said q third external terminals are coupled to said odd ones of said s second terminals.

Naito et al. teach the use of a capacitor comprising, m electrode plates; wherein each of said m electrode plates are arranged spaced apart in parallel; wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension, wherein w electrode plates of said m electrode plates comprise a second extension, wherein w is an integer less than m; n first external terminals; wherein n is an integer greater than 1; wherein said n first external terminals are arranged on a first common

exterior surface of said first capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals; wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals, s second external terminals, wherein s is an integer greater than 1; wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor, wherein said second extension of even ones of said w electrode plates are coupled to even ones of said s second external terminals, wherein said second extension of odd ones of said w electrode plates are coupled to odd ones of said s second external terminals.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form Li et al., using a plurality of capacitors of Naito et al., since such a modification would provide a group of capacitors in the system of Li et al.; and would provide a group of capacitors having a reduced series inductance.

*It should be noted Li et al. as modified by Naito et al. would produce a device having a first capacitor comprising, m electrode plates; wherein each of said m electrode plates are arranged spaced apart in parallel; wherein m is an integer greater than 1; wherein each of said m electrodes comprises a first extension, wherein w electrode plates of said m electrode plates comprise a second extension, wherein w is an integer less than m; n first external terminals; wherein n is an integer greater than 1; wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor, wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals; wherein said first

extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals, s second external terminals, wherein s is an integer greater than 1; wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor, wherein said second extension of even ones of said w electrode plates are coupled to even ones of said s second external terminals, wherein said second extension of odd ones of said w electrode plates are coupled to odd ones of said s second external terminals, the second capacitor comprising: x electrode plates, wherein each of said x electrode plates are arranged spaced apart in parallel; wherein x is an integer greater than 1; wherein y electrode plates of said x electrode plates comprise a third extension, wherein y is an integer less than x; q third external terminals, wherein q is an integer greater than 1, wherein said q third external terminals are arranged on a third common exterior surface of said second capacitor; wherein said third extension of even ones of said y electrode plates are coupled to even ones of said q third external terminals; wherein said third extension of odd ones of said y electrode plates are coupled to odd ones of said q third external terminals; wherein said second capacitor is disposed abutting and adjacent to said first capacitor, wherein said even ones of said q third external terminals are coupled to said even ones of said s second terminals; and wherein said odd ones of said q third external terminals are coupled to said odd ones of said s second terminals.

Regarding claim 62, Li et al. as modified by Naito et al. disclose z electrode plates of said m electrode plates comprise a fourth extension, wherein sum of y and z is integer less than or equal to m; wherein the first capacitor further comprises f fourth

external terminals; wherein f is an integer greater than 1, wherein said f fourth external terminals are arranged on a fourth common exterior surface of said first capacitor, wherein said fourth common exterior surface is opposite to said second common exterior surface; wherein said fourth extension of even ones of said z electrode plates are coupled to even ones of said f fourth external terminals; and wherein said third extension of odd ones of said z electrode plates are coupled to odd ones of said f fourth external terminals.

Regarding claim 77, Li et al. as modified by Naito et al. disclose an encapsulation encloses the device (fig. 13).

16. Claims 75-76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (US 6,636,416) and Naito et al. (US 6,072,687), as applied to claim 61 above, and further in view of DiFonzo et al. (US 6,262,886).

The modified Li et al. disclose the claimed invention except for a housing that encloses at least part of the first and second capacitors. Li et al. disclose the capacitors are used in a person computer.

DiFonzo et al. teach that it is known to use a housing for a computer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the capacitors (computer) of Li et al. in a housing as taught by DiFonzo et al., since such a modification would provide protection for the system of Li et al. (the capacitors of Li et al. (as modified by DiFonzo) are enclosed by a housing).

Regarding claim 76, DiFonzo et al. teach the claimed housing. Regarding the limitation, "the housing is formed from an ejection molding process" is a method of

forming the device. The method of forming the device is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight.

17. Claim 92 is rejected under 35 U.S.C. 103(a) as being unpatentable over Galvagni et al. (US 5,799,379) and DuPre et al. (US 6,243,253) as applied to claim 61 above, and further in view of Nagakari et al. (US 6,282,079).

The modified DuPre et al. disclose a system for the capacitor device wherein the electrodes are formed perpendicular to a substrate (70).

The modified DuPre et al. disclose the claimed invention except for the substrate is a printed circuit board.

Nagakari et al. teach that it is common to form capacitor on a printed circuit board.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the capacitor of the modified DuPre et al., on a printed circuit board, since such a modification would provide a capacitor of DuPre et al. in a system to operate, and would provide a printed circuit board with a capacitor having low inductance.

18. Claims 18-22, are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagakari et al. (US 6,282,079) in view of Iwanami (US 6,396,713).

Nagakari et al. disclose the claimed invention except for a system comprising an inductor; a capacitor of Claim 1, wherein said inductor is connected to even ones of said n first external terminals, wherein an output terminal is connected to even ones of said n

first external terminals, and wherein a reference voltage is connected to odd ones of said n first external terminals.

Iwanami teaches that it is known in the art to form a system where like polarity terminals are connected to reference voltage and output, an inductor is connected to one polarity of the external terminals of the capacitor.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to place the capacitor of Nagakari et al. in the Iwanami system, since such a modification would provide a capacitor for Iwanami, wherein the capacitor has low parasitic inductance.

*It should be noted that Nagakari et al. as modified by Iwanami discloses a system comprising an inductor; a capacitor of Claim 1, wherein said inductor is connected to even ones of said n first external terminals, wherein an output terminal is connected to even ones of said n first external terminals, and wherein a reference voltage is connected to odd ones of said n first external terminals.

Regarding claim 19, Nagakari et al. as modified by Iwanami discloses n=3; wherein said n first external terminals are arranged in parallel and wherein said even one of said n first external terminals is arranged between the odd ones of said n first external terminals, wherein first and third ones of said n first external terminals are coupled to the reference voltage, wherein one terminal of said inductor is coupled to a first end portion of a second one of said n first external terminals, and wherein the output terminal of said filter is provided at a second end portion of said second one of said n first external terminals.

Regarding claim 20, Nagakari et al. as modified by Iwanami discloses n=2; wherein said n first external terminals are arranged in parallel, wherein first one of said n first external terminals is coupled to a reference voltage; wherein one terminal of said inductor is coupled to a first end portion of a second one of said n first external terminals; and wherein an output terminal of said filter is provided at a second end portion of said second one of said n first external terminals.

Regarding claim 21, Nagakari et al. as modified by Iwanami discloses the claimed structure.

Regarding claim 22, Nagakari et al. as modified by Iwanami discloses a system comprising a multilayer printed circuit board (fig. 3); wherein said capacitor is mounted on said multilayer printed circuit board (13b); wherein said inductor (10) is connected to a first trace of said multilayer printed circuit board; wherein said first trace is connected to said even ones of said n first external terminals by way of a first plurality of vias; wherein said output terminal is connected to a second trace on said multilayer printed circuit board; wherein said second trace is connected to said even ones of said n first external terminals by way of a second plurality of vias; wherein the reference voltage is connected to a third trace on said multilayer printed circuit board; and wherein said third trace is connected to said odd ones of said n first external terminals by way of a third plurality of vias.

19. Claim 18, 19, 21, 82, 83 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahiko et al. (US 6,292,351) and Nagakari et al. (US 6,282,079) as applied to claim 1 above, and further in view of Iwanami (US 6,396,713).

Ahiko et al. disclose a capacitor formed on a printed circuit board (see fig. 4). The modified Ahiko et al. disclose the claimed invention except for a system comprising an inductor; a capacitor of Claim 1, wherein said inductor is connected to even ones of said n first external terminals, wherein an output terminal is connected to even ones of said n first external terminals, and wherein a reference voltage is connected to odd ones of said n first external terminals.

Iwanami teaches that it is known in the art to form a system where like polarity terminals are connected to reference voltage and output, an inductor is connected to one polarity of the external terminals of the capacitor.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to place the capacitor of modified Ahiko et al. in the Iwanami system, since such a modification would provide a capacitor for Iwanami; wherein the capacitor has low parasitic inductance.

*It should be noted that modified Ahiko et al. disclose a system comprising an inductor; a capacitor of Claim 1, wherein said inductor is connected to even ones of said n first external terminals, wherein an output terminal is connected to even ones of said n first external terminals, and wherein a reference voltage is connected to odd ones of said n first external terminals.

Regarding claim 19, the modified Ahiko et al. discloses n=3; wherein said n first external terminals are arranged in parallel and wherein said even one of said n first external terminals is arranged between the odd ones of said n first external terminals, wherein first and third ones of said n first external terminals are coupled to the reference

voltage, wherein one terminal of said inductor is coupled to a first end portion of a second one of said n first external terminals, and wherein the output terminal of said filter is provided at a second end portion of said second one of said n first external terminals.

Regarding claim 20, the modified Ahiko et al. discloses n=2; wherein said n first external terminals are arranged in parallel, wherein first one of said n first external terminals is coupled to a reference voltage; wherein one terminal of said inductor is coupled to a first end portion of a second one of said n first external terminals; and wherein an output terminal of said filter is provided at a second end portion of said second one of said n first external terminals.

Regarding claim 21, the modified Ahiko et al. discloses the claimed structure.

Regarding claim 82, the modified Ahiko et al. disclose the system further comprises a printed circuit board, wherein the m electrode plates of the capacitor are oriented perpendicular to the printed circuit board.

Regarding claim 83, the modified Ahiko et al. disclose the system further comprises a printed circuit board, wherein the m electrode plates of the capacitor are oriented perpendicular to the printed circuit board.

20. Claims 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda et al. (US 6,594,136) in view of Iwanami (US 6,396,713).

Kuroda et al. dislcose the claimed invention except for the capacitor is in a system comprising an inductor; wherein said inductor is connected to even ones of said n first external terminals, wherein an output terminal is connected to even ones of said n

first external terminals, and wherein a reference voltage is connected to odd ones of said n first external terminals.

Iwanami teaches that it is known in the art to form a system where like polarity terminals are connected to reference voltage and output, an inductor is connected to one polarity of the external terminals of the capacitor.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to place the capacitor of modified Kuroda et al. in the Iwanami system, since such a modification would provide a capacitor for Iwanami, wherein the capacitor has low parasitic inductance.

It should be noted the Kuroda et al. discloses a system comprising an inductor; a capacitor structure of Claim 24, wherein said inductor is connected to even ones of said n first external terminals, wherein an output terminal is connected to even ones of said n first external terminals, and wherein a reference voltage is connected to odd ones of said n first external terminals.

Regarding claim 38, the modified Kuroda et al. disclose n=3; wherein said n first external terminals are arranged in parallel and wherein said even one of said n first external terminals is arranged between the odd ones of said n first external terminals, wherein first and third ones of said n first external terminals are coupled to the reference voltage, wherein one terminal of said inductor is coupled to a first end portion of a second one of said n first external terminals, and wherein the output terminal of said filter is provided at a second end portion of said second one of said n first external terminals.

Regarding claim 39, the modified Kuroda et al. disclose said n first external terminals are arranged in parallel, wherein first one of said n first external terminals is coupled to a reference voltage; wherein one terminal of said inductor is coupled to a first end portion of a second one of said n first external terminals, and wherein an output terminal of said filter is provided at a second end portion of said second one of said n first external terminals.

Regarding claim 40, the modified Kuroda et al. disclose a device comprising a multilayer printed circuit board; wherein said capacitor structure is mounted on said multilayer printed circuit board; wherein said inductor is connected to a first trace of said multilayer printed circuit board; and wherein said first trace is connected to said even ones of said n first external terminals by way of a first plurality of vias; wherein said output terminal is connected to a second trace on said multilayer printed circuit board; wherein said second trace is connected to said even ones of said n first external terminals by way of a second plurality of vias; wherein the reference voltage is connected to a third trace on said multilayer printed circuit board; and wherein said third trace is connected to said odd ones of said n first external terminals by way of a third plurality of vias.

21. Claims 37, 40, 54-58, 86-87, 89-90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahiko et al. (US 6,292,351) in view of Iwanami (US 6,396,713).

Ahiko et al. disclose the claimed invention except for the capacitor is in a system comprising an inductor; wherein said inductor is connected to even ones of said n first external terminals, wherein an output terminal is connected to even ones of said n first

external terminals, and wherein a reference voltage is connected to odd ones of said n first external terminals.

Iwanami teaches that it is known in the art to form a system where like polarity terminals are connected to reference voltage and output, an inductor is connected to one polarity of the external terminals of the capacitor.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to place the capacitor of modified Ahiko et al. in the Iwanami system, since such a modification would provide a capacitor for Iwanami, wherein the capacitor has low parasitic inductance.

It should be noted the modified Ahiko et al. discloses a system comprising an inductor; a capacitor structure of Claim 24, wherein said inductor is connected to even ones of said n first external terminals, wherein an output terminal is connected to even ones of said n first external terminals, and wherein a reference voltage is connected to odd ones of said n first external terminals.

Regarding claim 38, the modified Ahiko et al. disclose n=3; wherein said n first external terminals are arranged in parallel and wherein said even one of said n first external terminals is arranged between the odd ones of said n first external terminals, wherein first and third ones of said n first external terminals are coupled to the reference voltage, wherein one terminal of said inductor is coupled to a first end portion of a second one of said n first external terminals, and wherein the output terminal of said filter is provided at a second end portion of said second one of said n first external terminals.

Regarding claim 39, the modified Ahiko et al. disclose said n first external terminals are arranged in parallel, wherein first one of said n first external terminals is coupled to a reference voltage; wherein one terminal of said inductor is coupled to a first end portion of a second one of said n first external terminals, and wherein an output terminal of said filter is provided at a second end portion of said second one of said n first external terminals.

Regarding claim 40, the modified Ahiko et al. disclose a device comprising a multilayer printed circuit board; wherein said capacitor structure is mounted on said multilayer printed circuit board; wherein said inductor is connected to a first trace of said multilayer printed circuit board; and wherein said first trace is connected to said even ones of said n first external terminals by way of a first plurality of vias; wherein said output terminal is connected to a second trace on said multilayer printed circuit board; wherein said second trace is connected to said even ones of said n first external terminals by way of a second plurality of vias; wherein the reference voltage is connected to a third trace on said multilayer printed circuit board; and wherein said third trace is connected to said odd ones of said n first external terminals by way of a third plurality of vias.

Regarding claim 54, Ahiko et al. disclose the claimed invention except for a system comprising: an inductor, wherein said inductor is connected to even ones of said n first external terminals, wherein an output terminal is connected to even ones of said n first external terminals, and wherein reference voltage is connected to odd ones of said n first a external terminals.

Iwanami teaches that it is known in the art to form a system where like polarity terminals are connected to reference voltage and output, an inductor is connected to one polarity of the external terminals of the capacitor.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to place the capacitor of modified Ahiko et al. in the Iwanami system, since such a modification would provide a capacitor for Iwanami, wherein the capacitor has low parasitic inductance.

It should be noted the modified Ahiko et al. discloses a system comprising an inductor; a capacitor structure of Claim 41, wherein said inductor is connected to even ones of said n first external terminals, wherein an output terminal is connected to even ones of said n first external terminals, and wherein a reference voltage is connected to odd ones of said n first external terminals.

Regarding claim 55, the modified Ahiko et al. discloses n=3; wherein said n first external terminals are arranged in parallel and wherein said even one of said n first external terminals is arranged between the odd ones of said n first external terminals, wherein first and third ones of said n first external terminals are coupled to the reference voltage, wherein one terminal of said inductor is coupled to a first end portion of a second one of said n first external terminals, and wherein the output terminal of said filter is provided at a second end portion of said second one of said n first external terminals.

Regarding claim 56, the modified Ahiko et al. disclose n=2; wherein said n first external terminals are arranged in parallel; wherein first one of said n first external

terminals is coupled to a reference voltage, wherein one terminal of said inductor is coupled to a first end portion of a second one of said n first external terminals; and wherein an output terminal of said filter is provided at a second end portion of said second one of said n first external terminals.

Regarding claim 57, the modified Ahiko et al. disclose a system comprising a multilayer printed circuit board; wherein said capacitor structure is mounted on said multilayer printed circuit board; wherein said inductor is connected to a first trace of said multilayer printed circuit board; and wherein said first trace is connected to said even ones of said n first external terminals by way of a first plurality of vias; wherein said output terminal is connected to a second trace on said multilayer printed circuit board; wherein said second trace is connected to said even ones of said n first external terminals by way of a second plurality of vias; wherein the reference voltage is connected to a third trace on said multilayer printed circuit board; and wherein said third trace is connected to said odd ones of said n first external terminals by way of a third plurality of vias.

Regarding claim 58, the modified Ahiko et al. disclose s=1; wherein said s second external terminal is coupled to even ones of said m electrode plates; and wherein said s third external terminal is coupled to even ones of said x electrode plates.

Regarding claim 86, the modified Ahiko et al. disclose the system further comprises a printed circuit board, wherein the m electrode plates of the capacitor are oriented perpendicular to the printed circuit board.

Regarding claim 87, the modified Ahiko et al. disclose the system further comprises a printed circuit board, wherein the m electrode plates of the capacitor are oriented perpendicular to the printed circuit board.

Regarding claim 89, the modified Ahiko et al. disclose the system further comprises a printed circuit board, wherein the m electrode plates of the capacitor are oriented perpendicular to the printed circuit board.

Regarding claim 90, the modified Ahiko et al. disclose the system further comprises a printed circuit board, wherein the m electrode plates of the capacitor are oriented perpendicular to the printed circuit board.

22. Claims 25, and 80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (US 6,636,416) and Naito et al. (US 6,072,687) in further view of Houghton et al. (US 6,282,095).

Li et al. disclose the claimed invention except for the housing that partially encloses the first and second capacitor

Houghton et al. teach (fig. 4) that it is common in the art to form a housing around an electrical component.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the capacitor of Li et al. by forming a housing around the electrical component, since such a modification would provide a protective housing with excellent heat dissipation around the electronic component.

Regarding claim 80, Houghton et al. disclose the housing comprises a fin to dissipated heat.

***Conclusion***

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

4,853,826; 2003/0030510; US 2004/0174656 – all disclose a capacitor having the same claimed capacitor.

2004/0066603 – a multilayer capacitor having separate unit capacitor connected in parallel.

In order to ensure full consideration of any amendments, affidavits, or declaration, or other documents as evidence of patentability, such documents must be submitted in response to this Office action. Submissions after the next Office action, which is intended to be a final action, will be governed by the requirements of 37 CFR 1. 116 which will be strictly enforced.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric W Thomas whose telephone number is 571-272-1985. The examiner can normally be reached on M,Tu,Sat 9 am - 9:30 pm; W, Th, F 6 pm -10:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eric W Thomas 9/17/04
Examiner
Art Unit 2831

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